

THE MANAGEMENT DEVELOPMENT OF CHINESE ARCHITECTURAL DESIGN CHIP ENTERPRISES BASED ON COMPARATIVE ADVANTAGE FEATURES

Liu Fang¹, Pichai Sodphiban²

College of Art, Bangkok Thonburi University ¹⁻²
China,¹ Thailand²

Email: lf13515029593@163.com¹, vivan898@hotmail.com²

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Abstract

Against the backdrop of the China US trade friction, the importance of management and development of China's architectural design chip enterprises has risen to the level of national strategic security. Evaluating the performance of China's architectural design chip enterprises through scientific and objective methods is not only beneficial for identifying their development advantages, but also for the government to efficiently allocate resources to these enterprises. Therefore, based on the characteristics of architectural design chip enterprises, a performance evaluation method for Chinese architectural design chip enterprises based on comparative advantage features was developed, and combined with the established indicator evaluation system applicable to architectural design chip enterprises, applied research was conducted on 9 listed architectural design chip enterprises in China. Finally, based on the evaluation results and combined with the current national conditions in China, reasonable countermeasures are proposed for the future development of China's architectural design chip enterprises.

Keywords: Management development; Architectural design; Chip enterprises; Comparative advantage features

Introduction

With the rapid development of global technological innovation, the chip industry has become a key force driving modern economic and technological progress. Especially in the field of architectural design, the increasingly widespread application of chip technology has promoted the rapid development of innovative methods such as Building Information Modeling (BIM), intelligent buildings, 3D modeling and rendering, and building performance simulation. Architectural design chips help architects and engineers optimize design schemes, improve construction efficiency, and promote intelligent and green development in the field of architecture through efficient data processing and simulation analysis. At the same time, the rapid development of artificial intelligence, the Internet of Things, and 5G communication technology has also provided new opportunities for innovation in architectural design chips, making them have broad market prospects in emerging fields such as smart cities and smart homes. China is one of the world's largest construction markets, and the rapid development of the construction industry has raised higher technological demands for architectural design chips. However, although China's chip industry has made progress in some fields, especially in consumer electronics and communication chips, chip technology in the field of architectural design still lags behind the international advanced level. In the international market, the core of architectural design chip technology is still dominated by a few large enterprises from countries such as the United States, Europe, and Japan, especially in the research and manufacturing of high-end architectural design chips. Chinese enterprises have not yet formed an independent innovation technology system. In summary, based on the development trend of China's architectural design chip enterprises, a comparative advantage-based approach has been developed.

Management Development of Chinese

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buildings, 3D modeling and rendering, and building performance simulation. Architectural design chips help architects and engineers optimize design schemes, improve construction efficiency, and promote intelligent and green development in the field of architecture through efficient data processing and simulation analysis. At the same time, the rapid development of artificial intelligence, the Internet of Things, and 5G communication technology has also provided new opportunities for innovation in architectural design chips, making them have broad market prospects in emerging fields such as smart cities and smart homes. China is one of the world's largest construction markets, and the rapid development of the construction industry has raised higher technological demands for architectural design chips. However, although China's chip industry has made progress in some fields, especially in consumer electronics and communication chips, chip technology in the field of architectural design still lags behind the international advanced level. In the international market, the core of architectural design chip technology is still dominated by a few large enterprises from countries such as the United States, Europe, and Japan, especially in the research and manufacturing of high-end architectural design chips. Chinese enterprises have not yet formed an independent innovation technology system.

Architectural Design

Currently, the international chip industry is facing increasingly fierce technological competition, especially the intensification of trade frictions between China and the United States, which has made the technological bottleneck in China's semiconductor industry more prominent. The United States and its allies have imposed a series of sanctions on China's high-tech industry, causing some important architectural design chip companies to encounter numerous difficulties in technology research and market development. As one of the world's largest chip demand markets, China's annual import of chips is close to 300 billion US dollars, and chips have become a key factor in national strategic security and industrial competitiveness. As a part of high-end chips, architectural design chips shoulder the responsibility of promoting modernization and intelligence in the construction industry. Their technological breakthroughs are of great significance for the innovative transformation of China's construction industry. Based on the above

background, this article will use the theory of comparative advantage to study the current development status of China's architectural design chip enterprises. By analyzing the competitive advantages and disadvantages of China in the field of architectural design chips, combined with the domestic and international market environment and technological development trends, this article proposes a performance evaluation method for architectural design chip enterprises based on comparative advantage characteristics. This method will help identify the core competitiveness of Chinese architectural design chip companies and provide theoretical support for their positioning and development in the global market. In addition, based on the evaluation results and combined with China's national conditions and industrial policies, this article will propose practical and feasible development strategies to promote the independent innovation and international competitiveness of China's architectural design chip industry.

A Comprehensive Performance Evaluation Method for Chinese Architectural Design Chip Enterprises Based on Comparative Advantage Features

The evaluation index system of an architectural design chip enterprise is composed of a K-dimensional vector, denoted as $X = (x_1, x_2, \dots, x_k)^T$. Each dimension x_i represents a specific evaluation index that measures an aspect of the enterprise's performance. For simplicity, it is assumed that a larger value of an evaluation index corresponds to better performance. However, in cases where a smaller value indicates better performance, the index can be adjusted or inversed during the standardization process to align with the assumption that "larger is better." This ensures consistency across all indices and facilitates comparison.

In addition to the primary evaluation indices, secondary evaluation indices can be established or extended based on the specific needs and characteristics of the evaluation system. These secondary indices ($i=1, 2, \dots, k_i=1, 2, \dots, k$) allow for greater flexibility and granularity in the assessment, enabling evaluators to capture nuanced aspects of performance that are relevant to architectural design chip enterprises.

Once the evaluation indices are defined, the n organizations participating in the evaluation are represented by their respective performance vectors

X_1, X_2, \dots, X_n . Each vector encapsulates the performance values across all evaluation indices for a particular organization. To enable meaningful comparisons across organizations, the data is standardized. Standardization ensures that all indices, regardless of their original scales or units, are normalized and contribute equally to the evaluation process.

To determine the preferred outcomes for each evaluation index, the preference outcomes of all sub-indicators are summarized and represented as $X^* = (x_1^*, x_2^*, \dots, x_k^*)^T$. These preference outcomes serve as benchmarks against which the performance of each organization is measured. There are three widely recognized approaches to determining these preferred outcomes:

Actual Ideal Outcome: This approach selects the best observed performance for each evaluation index among all the participating organizations. It represents a realistic benchmark because it is derived directly from actual performance data. This method reflects the best achievable outcomes under real-world conditions and is therefore considered the most practical and objective for many applications.

Ideal Best Outcome: This method sets the benchmark based on theoretically optimal values for each evaluation index. These values may not necessarily be observed in the actual data but represent an aspirational target. This approach is often used in scenarios where achieving the theoretical best is the ultimate goal, such as in long-term strategic planning.

Expanding Ideal Outcome: This method creates an extended benchmark by further enhancing the best observed values or theoretical values. It is designed to encourage continuous improvement by setting challenging targets that go beyond current or theoretical best performance levels.

Given the unique characteristics of architectural design chip enterprises and the emphasis on objectivity in this study, the Actual Ideal Outcome is chosen as the optimal outcome for the evaluation. Specifically, the actual ideal result x_i^* is defined as the best observed value for each individual evaluation index i , where $i = 1, 2, \dots, k$. These individual optimal values are then aggregated to form the actual ideal outcome

vector, denoted as $X^*=(x_1^*,x_2^*,\dots,x_k^*)TX^* = (x_1^*, x_2^*, \dots, x_k^*)^T$. This vector serves as a realistic and achievable benchmark, reflecting the best performance observed across all participating organizations for each evaluation index.

By adopting the actual ideal outcome approach, the evaluation process remains grounded in reality, leveraging concrete data to identify top performers and establish performance benchmarks. This methodology not only enhances the objectivity and reliability of the evaluation system but also provides actionable insights that organizations can use to improve their performance in the context of architectural design chip enterprises.

Comparative Advantage Characteristics Evaluation of Performance of Architectural Design Chip Enterprises in China

Data source and processing: Based on the extended BSC evaluation index system, this article selected 9 enterprises in China's chip industry as research objects and collected relevant evaluation index values for each enterprise, as shown in Table 2. Due to the comprehensive evaluation of architectural design chip enterprises from multiple perspectives, the non-identical dimensions of various indicators can result in significant differences in the original data levels between indicators. For the convenience of subsequent data processing and calculation, the raw data in Table 1 is standardized to eliminate the influence of dimensions between different indicators.

Table 1: Original Data Units of Performance of 9 Architectural Design Chip Enterprises in China.

corpor ation	X ₁				X ₂			X ₃			X ₄			X ₅	
	X ₁₁	X ₁₂	X ₁₃	X ₂₁	X ₂₂	X ₃₁	X ₃₂	X ₃₃	X ₄₁	X ₄₂	X ₄₃	X ₅₁	X ₅₂		
A	647325.00	231736.00	35.99	0.86	73.95	107906.13	101	16.67	2	0	0	1478	50.09		
B	2201788.29	179376.42	8.15	2.88	0.00	481158.30	631	21.85	3	2	2	2530	20.53		
C	343041.00	40576.00	9.69	0.50	39.54	57547.00	70	16.78	2	1	0	1133	31.48		
D	2352628.00	8866.00	0.70	3.11	0.00	96875.42	144	4.12	0	0	3	5785	0.00		
E	9073658.00	514788.00	14.67	12.00	6.11	1254790.00	1000	13.83	3	2	0	28301	33.70		

F	810349.00	28679.00	3.69	1.10	13.79	40211.00	36	4.96	0	0	2	4323	0.72
G	428056.00	6760.00	1.96	0.60	37.61	42589.48	114	13.69	2	1	1	2345	7.40
H	3514781.00	128054.00	7.95	4.60	47.99	202282.45	738	5.76	1	2	0	16911	3.68
I	826657.00	1914.00	0.31	1.09	14.45	70529.89	23	8.53	0	0	3	3975	1.47

Data source: Guotai An Database, 2023 Annual Financial Reports of Listed Companies, <https://www.gtarsc.com/> 2. Giant Tide Information Network, <http://www.cninfo.com.cn/new/index> 3. The data of Company B comes from the Hong Kong Stock Exchange in 2023, which is in thousands of US dollars. This article converts it into RMB (10000 yuan) based on the exchange rate of US dollars to RMB on December 31, 2023 (the exchange rate of US dollars to RMB on that day was: 1 US dollar=6.9762 yuan, for ease of calculation, 1 US dollar=7 yuan).

Table 2: Evaluation Index Data of Performance Standardization Processing for 9 Architectural Design Chip Enterprises in China.

	X₁			X₂		X₃			X₄		X₅		
corp	X₁₁	X₁₂	X₁₃	X₂₁	X₂₂	X₃₁	X₃₂	X₃₃	X₄₁	X₄₂	X₄₃	X₅₁	X₅₂
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A	0.035	0.448	1.000	0.031	1.000	0.056	0.080	0.708	0.667	0.000	0.000	0.013	1.000
B	0.213	0.346	0.220	0.207	0.000	0.363	0.622	1.000	1.000	1.000	0.667	0.051	0.410
C	0.000	0.075	0.263	0.000	0.535	0.014	0.048	0.714	0.667	0.500	0.000	0.000	0.628
D	0.230	0.014	0.011	0.227	0.000	0.047	0.124	0.000	0.000	0.000	1.000	0.171	0.000
E	1.000	1.000	0.402	1.000	0.083	1.000	1.000	0.548	1.000	1.000	0.000	1.000	0.673
F	0.054	0.052	0.095	0.052	0.186	0.000	0.013	0.047	0.000	0.000	0.667	0.117	0.014
G	0.010	0.009	0.046	0.009	0.509	0.002	0.093	0.540	0.667	0.500	0.333	0.045	0.148
H	0.363	0.246	0.214	0.357	0.649	0.133	0.732	0.092	0.333	1.000	0.000	0.581	0.073
I	0.055	0.000	0.000	0.051	0.195	0.025	0.000	0.249	0.000	0.000	1.000	0.105	0.029

Using Matlab and SPSS computing tools, the standardized performance data of 9 architectural design chip enterprises in China were processed. According to the performance evaluation method based on comparative advantage features developed in this article, the following tables were obtained. (Table 4, Table 5, Table 6, Table 7)

Table 3: Comparative Advantage Value Parameters (i.e. Weight Coefficients) of Performance of 9 Architectural Design Chip Enterprises in China (Second Level Indicators)

corporation	X ₁	X ₂	X ₃	X ₄	X ₅
A	0.3333	0.3333	0.0000	0.0000	0.3333
B	0.0000	0.0000	0.3333	0.6667	0.0000
C	0.0867	0.1215	0.3106	0.3028	0.1783
D	0.0000	0.0000	0.0000	1.0000	0.0000
E	0.2500	0.1250	0.2500	0.2500	0.1250
F	0.1532	0.1165	0.1390	0.4885	0.1027
G	0.0952	0.1565	0.2106	0.4627	0.0750
H	0.0000	0.0000	0.0000	1.0000	0.0000
I	0.0000	0.0000	0.0000	1.0000	0.0000

Table 4: Comparative Advantage Value Parameters (i.e. Weight Coefficients) of Performance of 9 Architectural Design Chip Enterprises in China (Second Level Indicators).

corporation	X ₁₁	X ₁₂	X ₁₃	X ₂₁	X ₂₂	X ₃₁	X ₃₂	X ₃₃	X ₄₁	X ₄₂	X ₄₃	X ₅₁	X ₅₂
A	0.0000	0.0000	1.0000	0.0000	1.0000	0.0800	0.0843	0.8357	0.8182	0.0909	0.0909	0.0000	1.0000
B	0.2885	0.4179	0.2936	0.6139	0.3861	0.0000	0.0000	1.0000	0.5000	0.5000	0.0000	0.2790	0.7210
C	0.2494	0.2917	0.4590	0.1780	0.8220	0.0717	0.0768	0.8515	0.6429	0.2857	0.0714	0.1213	0.8787
D	0.4515	0.2750	0.2735	0.6259	0.3741	0.3233	0.3828	0.2939	0.0000	0.0000	1.0000	0.5928	0.4072
E	0.5000	0.5000	0.0000	1.0000	0.0000	0.5000	0.5000	0.0000	0.5000	0.5000	0.0000	1.0000	0.0000
F	0.3236	0.3227	0.3537	0.4242	0.5758	0.3196	0.3283	0.3522	0.0909	0.0909	0.8182	0.5550	0.4450
G	0.3249	0.3248	0.3503	0.1973	0.8027	0.1446	0.1752	0.6802	0.5902	0.2623	0.1475	0.4431	0.5569
H	0.4220	0.3009	0.2770	0.2294	0.7706	0.0809	0.8452	0.0738	0.0000	1.0000	0.0000	0.8301	0.1699
I	0.3591	0.3204	0.3204	0.4184	0.5816	0.2751	0.2615	0.4634	0.0000	0.0000	1.0000	0.5403	0.4597

Table 5: Democratic evaluation results of performance (top-level indicators) of 9 architectural design chip enterprises in China

angel	A	B	C	D	E	F	G	H	I
dj _A	0.0000	0.4663	0.3159	0.5753	0.3809	0.5220	0.4567	0.4215	0.5364

dj,C	0.1435	0.1453	0.1471	0.3922	0.1624	0.3788	0.2138	0.3154	0.3449
dj,D	1.0000	0.3333	1.0000	0.0000	1.0000	0.3333	0.6667	1.0000	0.0000
dj,E	0.3062	0.2209	0.3086	0.3193	0.0000	0.3411	0.3071	0.2103	0.3433
dj,F	0.4174	0.1814	0.4214	0.1635	0.4066	0.2107	0.3023	0.4152	0.1628
dj,G	0.1859	0.1441	0.1689	0.3649	0.1508	0.3566	0.1742	0.2473	0.3459
dj,H	1.0000	0.0000	0.5000	1.0000	0.0000	1.0000	0.5000	0.0000	1.0000
dj,I	1.0000	0.3333	1.0000	0.0000	1.0000	0.3333	0.6667	1.0000	0.0000
$1/9 \sum dj$	0.4908	0.2027	0.4537	0.3769	0.3613	0.4494	0.3933	0.4428	0.3630
Sort	9	1	8	4	2	7	5	6	3

Table 6: Comparative Advantage Ranking of Performance (Top Level Indicator) of 9 Architectural Design Chip Enterprises in China.

Sort	dj,A	dj,B	dj,C	dj,D	dj,E	dj,F	dj,G	dj,H	dj,I
1	★	★	A	★	★	I	B	B	D
2	C	E	B	I	H	D	E	E	▲
3	E	C	▼	B	B	B	C	▼	B
4	H	G	E	F	A	▼	▼	C	F
5	G	A	G	G	G	G	A	G	G
6	B	H	H	A	C	E	H	A	A
7	F	I	I	C	D	H	I	D	C
8	I	F	F	E	F	A	F	F	E
9	D	D	D	H	I	C	D	I	H

Analysis of evaluation results

(1) In Table 4, each architectural design chip enterprise has different value parameters (weight coefficients) corresponding to different indicators, indicating that the advantages of each enterprise are different and highlighting their respective characteristics. The larger the value parameter, the more obvious the advantage of the enterprise in that aspect. Taking architectural design chip enterprise B as an example, its (second level indicator) value parameter is $W = (0.0000, 0.0000, 0.3333, 0.6667, 0.0000)$, indicating that its comparative advantage lies in two aspects: internal business processes and innovation, with

the internal business processes being the most prominent, and the value parameter being 0.6667. According to Table 4 (three-layer indicators), the main influencing factors of X4 weight for Company B are X41, X42, and X43, with value parameters $W = (0.5000, 0.5000, 0.0000)$, indicating that Company B's advantage in internal business processes is due to its outstanding chip design and production capabilities. Therefore, when evaluating the performance of the evaluated organization, standing from the perspective that is most beneficial to the evaluated architectural design chip enterprise is more conducive to exploring and leveraging its comparative advantage characteristics.

(2) In Table 6, among the nine selected architectural design chip companies in China, companies A, B, D, and E ranked in the top 10% due to their ability to evaluate themselves from the most favorable perspective. Therefore, the performance of architectural design chip companies A, B, D, and E has significant comparative advantages within this evaluation range, and the government should encourage their development characteristics. For architectural design chip company B, regardless of who evaluates it from, its performance is generally among the top and outstanding. Therefore, it can be said that Company B is widely recognized as an excellent enterprise for development, indicating that its development model has been recognized by several other companies. From the above analysis, it can be inferred that enterprise should develop their own characteristics and maintain deepening. The government should encourage architectural design chip companies with their development expertise and in line with public awareness, and provide relevant support to promote their performance improvement and development progress.

(3) Among the 9 selected architectural design chip companies in China, Company I only have certain advantageous performance characteristics, and does not have significant comparative advantage characteristics evaluated from its own perspective like A, B, D, and E. This indicates that even if some architectural design chip companies evaluate themselves from the most favorable perspective, it does not necessarily mean that they are the best. This also demonstrates the scientific and objective nature of the evaluation method developed in this article. It also indicates that under the evaluation model advocated by architectural design chip company I, there are better companies than themselves. Through analysis, it can be inferred that evaluation methods based on comparative advantage features are not only scientific, objective, and

fair, but also conducive to identifying and generating benchmark effects. Therefore, for architectural design chip enterprises with certain comparative advantages, while the enterprises themselves are benchmarking and learning progress, the government should also provide certain support to promote their rapid incubation and growth.

(4) Among the 9 selected architectural design chip companies in China, the performance advantages of companies C, F, G, and H are not obvious. This indicates that.

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New Knowledges

Based on the comparative advantage feature performance evaluation method developed in this article and the analysis results of the performance evaluation index system for architectural design chip enterprises constructed, combined with the current development status of Chinese enterprises and the complex domestic and international environment they face, the following new countermeasures and suggestions are proposed for the future development of Chinese architectural design chip enterprises.

Interactive and coordinated development to enhance self-sufficiency:

From the X41, X42, and X43 value parameters of each architectural design chip enterprise in Table 5, it can be seen that each enterprise has its own advantages in the three-key links of chip design, production, and packaging testing. However, considering the pain caused by the sanctions imposed by the US government and enterprises on China's architectural design chip companies in recent years, it can be seen that the development of various links in China's architectural design chip companies is uneven (for example, H company only focuses on chip packaging and testing, and has not reached the international level), and has not yet formed a complete and advanced chip industry chain. Compared to Japan after World War II, its domestic semiconductor industry has a well-established design, production, and packaging testing industry chain, effectively responding to strong pressure from the United States.

Strengthen R&D investment and attach importance to talent reserve: According to the results of the democratic proxy evaluation in Table 6, companies B and E are widely recognized as excellent enterprises. From Table 2, it can be seen that the R&D investment of enterprises B and E is relatively large, with enterprise E having the highest investment of 12547.9 million yuan. And both companies attach great importance to talent reserve and talent quality. For example, the proportion of employees with a master's degree or above in Company B is 20.53%, and the proportion of employees with a master's degree or above in Company E is 33.7%. It indicates that excellent enterprises within this evaluation scope attach great importance to research and development investment and talent reserves. Therefore, as a talent and technology intensive architectural design chip enterprise, it is necessary to increase research and development investment, introduce senior talents from home and abroad, strengthen talent reserves, and thus master core competitiveness in order to continuously develop and grow.

Create research portfolios to achieve catch-up innovation: According to Table 5, The value parameters of Company I (X41, X42, X43) are (0.0000, 0.0000, 1.0000), indicating that Company I mainly excels in the chip packaging and testing process. According to the analysis results in Table 2, only two companies, B and E, have reached the international level in the chip design process, and only companies D and I have reached the international level in the chip packaging and testing process. However, there are no domestic companies that can reach the

international level in the chip production process. In response to this issue, the government should take the lead in developing an organic combination of excellent enterprises in every aspect of chip design, production, packaging, and testing (such as the organic combination of design, B, and E enterprises). The government should also mobilize efficient scientific research talents in relevant fields to join the research team, and provide certain financial and policy support. At the same time, in the process of combination, it is also necessary to handle the relationship between "pre competition cooperation" and "post cooperation competition", improve the development quality of each link, and promote the rapid progress of China's chip industry, achieving catching up with the world's chip giants.

Conclusions

This article is based on the current domestic and international environment and specific development status of architectural design chip enterprises, using an expanded balanced scorecard as the evaluation index system, and utilizing the organizational performance evaluation method of Chinese architectural design chip enterprises based on comparative advantage characteristics. Nine Chinese architectural design chip enterprises were selected for application research, and their performance was scientifically and objectively evaluated. High performance enterprises were selected, and their excellent internal reasons were analyzed in depth. Finally, based on the practical background and evaluation results, reasonable countermeasures were proposed for the development of China's architectural design chip enterprises, providing relevant references and inspirations for the future development of China's architectural design chip enterprises.

References

- Binyamin, S., & Hoque, R. (2020). **Understanding the drivers of wearable health monitoring technology: An extension of the unified theory of acceptance and use of technology**. MOPI 12 (9605), pp. 1-20.
- Bolotin E, Cidon I, Ginosar R, et al. QNoC. (2004) **QoS architecture and design process for network on chip** [J]. Journal of systems architecture, 50(2-3), pp. 105-128.
- Rózanowski K, Sondej T. (2013). **Architecture design of the high integrated System-on-Chip for biomedical applications**[C]//Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems-MIXDES 2013. IEEE, pp. 529-533.
- Bertozzi D, Benini L. Xpipes. (2004). **A network-on-chip architecture for gigascale systems-on-chip**[J]. IEEE circuits and systems magazine, 4 (2), pp. 18-31.
- Bertozzi D, Benini L. Xpipes. (2004). **A network-on-chip architecture for gigascale systems-on-chip**[J]. IEEE circuits and systems magazine, 4(2), pp. 18-31.
- Mohanty S P, Gomathisankaran M, Kougianos E. (2014). **Variability - aware architecture level optimization techniques for robust nanoscale chip design** [J]. Computers & Electrical Engineering, 40(1), pp. 168-193.
- Liu, J., & Sun, H. (2020). **Addressing the urban-rural divide in music education**. Educational Research Review, 29(4), pp. 47-62.
- Wang, L., & Lee, C. (2016). **The impact of integrated music education on early childhood cognitive development**. Journal of Early Childhood Research, 14(2), pp. 112-128.
- Zhao, M. (2018). **Music education in China: Current trends and future directions**. Music Education Review, 56(3), pp.215-230.
- Zuk, J., Benjamin, C., Kenyon, A., & Gaab, N. (2014). **Behavioral and neural correlates of executive functioning in musicians and non-musicians**. PLoS One, 9(6), e99868.